REMARKS

Claims 12, 21, 22, 53, 56, 57 and 58 are amended. Claims 48-50 are canceled. Claims 12, 13, 16, 21-23, 47, 53 and 56-63 are in the application for consideration.

Claims 53 and 56-58 are rewritten in independent form, with the subject matter thereof previously having been indicated to be allowable by the Examiner. Accordingly, formal allowance of these claims is urged.

Claim 12 is amended to correct a typographical error, and otherwise for clarification.

Independent claim 21 stands rejected as being unpatentable over Crotti. Claim 21 has been amended to recite that the plug uppermost surface is outwardly exposed over the diffusion region during the beveling. Crotti clearly does not disclose or suggest the same as its allegedly equivalent plug material 7 between the illustrated conductive lines is covered with insulative material 8 during the alleged equivalent beveling. Accordingly, Crotti does not disclose or suggest that which Applicant now recites in independent claim 21. Accordingly, formal allowance thereof is requested.

Independent claim 22 is amended to recite that the first uppermost surface of the conductive plug which is referred to is that over the node location, and that the etching is of material of the conductive plug through such uppermost surface over the node location. Crotti clearly does not disclose or suggest such, as its uppermost surface of its allegedly equivalent conductive plugging material 7

is covered by insulative material 8, and therefore not etched therethrough. Crotti clearly does not disclose or suggest that which Applicant recites in amended claim 22. Accordingly, formal allowance thereof is requested.

Applicant's remaining dependent claims which have been rejected over Crotti should be allowed as depending from allowable base claims, and for their own recited features which are neither shown nor suggested in the cited art. Action to that end is requested. This application is believed to be in immediate condition for allowance, and action to that end is requested.

Respectfully submitted,

Dated: 8/21/02

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/909,111
Filing Date ..... July 18, 2001
Inventor ..... Mark Fischer, et al.
Assignee ..... Micron Technology, Inc.
Group Art Unit 1765
Examiner ..... Duy Deo
Attorney's Docket No. MI22-1777
Title: Semiconductor Processing Methods of Forming a Conductive Projection and Methods of Increasing Alignment Tolerances

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING PRELIMINARY AMENDMENT RESPONSE TO JUNE 14, 2002 OFFICE ACTION TO ACCOMPANY RCE FILING

In the Claims

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

12. (Thrice Amended) A method of forming DRAM circuitry comprising:

forming a conductive plug over a substrate node location between a pair of conductive lines and with which electrical communication with a bit line is desired, the conductive plug having a first uppermost surface; and

unevenly removing material from the first uppermost surface of the conductive plug without using masking material over the first uppermost surface between the pair of conductive lines to define an uneven second uppermost surface at least a portion of which is disposed elevationally higher than the

conductive lines and to reduce a width of the conductive plug from what it was prior to said unevenly removing.

21. (Twice Amended) A method of increasing alignment tolerances between bit line contact material and storage capacitors in a DRAM comprising beveling at least one corner of a conductive plug formed over a diffusion region with which a bit line is to electrically communicate effectively to reduce a width of the conductive plug, the beveling changing a first generally even uppermost surface of the conductive plug to a second generally uneven uppermost surface, the plug uppermost surface being outwardly exposed over the diffusion region during the beveling.

22. (Thrice Amended) A method of forming DRAM circuitry comprising:

forming a conductive plug over a substrate node location between a pair of conductive lines and with which electrical communication with a bit line is desired, the conductive plug having a first uppermost surface over the node location having a generally uniform surface and having a width terminating over respective conductive lines of the pair of conductive lines; and

etching material of the conductive plug through the first uppermost surface to define a second uppermost surface which is generally non-planar and at least a portion of which is disposed elevationally higher than the conductive lines and to reduce the width of the conductive plug.

Cancel claims 48-50.

53. (Amended) ~~The method of claim 21~~ A method of increasing alignment tolerances between bit line contact material and storage capacitors in a DRAM comprising beveling at least one corner of a conductive plug formed over a diffusion region with which a bit line is to electrically communicate effectively to reduce a width of the conductive plug, the beveling changing a first generally even uppermost surface of the plug to a second generally uneven uppermost surface, wherein the beveling is effective to reduce a height of the conductive plug over the diffusion region.

56. (Amended) ~~The method of claim 48~~ A semiconductor processing method of forming integrated circuitry comprising:

forming a pair of spaced and adjacent conductive contact projections over a substrate, the conductive contact projections having respective widths and a generally even first uppermost surface;

etching at least one of the conductive contact projections effective to reduce its width, and form a generally uneven second uppermost surface;

forming insulative material over the conductive contact projections after the etching;

etching at least one contact opening through the insulative material to at least one of the conductive contact projections proximate the other of the conductive contact projections; and

wherein the one projection has an uppermost surface and the etching of the one projection etches material of the one projection from an entirety of the uppermost surface.

57. (Amended) ~~The method of claim 48~~ A semiconductor processing method of forming integrated circuitry comprising:

forming a pair of spaced and adjacent conductive contact projections over a substrate, the conductive contact projections having respective widths and a generally even first uppermost surface;

etching at least one of the conductive contact projections effective to reduce its width, and form a generally uneven second uppermost surface;

forming insulative material over the conductive contact projections after the etching;

etching at least one contact opening through the insulative material to at least one of the conductive contact projections proximate the other of the conductive contact projections; and

wherein at least the one projection has an uppermost surface which is substantially planar immediately prior to the etching of the one projection.

58. (Amended) ~~The method of claim 48~~ A semiconductor processing method of forming integrated circuitry comprising:

forming a pair of spaced and adjacent conductive contact projections over a substrate, the conductive contact projections having respective widths and a generally even first uppermost surface;

etching at least one of the conductive contact projections effective to reduce its width, and form a generally uneven second uppermost surface;

forming insulative material over the conductive contact projections after the etching;

etching at least one contact opening through the insulative material to at least one of the conductive contact projections proximate the other of the conductive contact projections; and

wherein the conductive projections have outermost surfaces which are entirely outwardly exposed during the etching of the at least one projection.

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